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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,846	12/04/2003	Chien-An Yu	10113381	7437

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EXAMINER	
DAHIMENE, MAHMOUD	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,846	YU, CHIEN-AN	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments/Remarks

1. Applicant's arguments, see applicant's remarks, filed 1/27/2006, with respect to the rejection(s) of claim(s) 1-20 under 35 U.S.C. 103(a) have been fully considered, and with respect to the argument regarding the cited references failing to explicitly teach "etching the exposed substrate to form a recess region in the substrate" are convincing. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shimizu (US 2003/0143815).

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 2 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Shimizu (US 2003/0143815).

The reference of Shimizu discloses a method for fabricating a semiconductor device capable of preventing generation of a leakage current, two oxidation steps are used. The method uses rounding the top corner of a trench, comprising the steps of:

forming a masking layer including layers (103) and (104) (figure 3) overlying a substrate, patterning the masking layer to form at least one opening therein to expose the substrate (figure 3),

and etching the exposed substrate to form a recess region (101h) in the substrate (figure 3);

oxidizing the recess region to form a first oxide layer (105 s and 105b) (figure 4) thereon to round the top corner (105s) of the recess region (101h);

successively etching the first oxide layer (105b) (figure 5) and the substrate under the opening (107) (figure 5) to form the trench (107) in the substrate , and

conformably forming a second oxide layer (115) (figure 7) on the surface of the trench (107) (see also page 3, paragraphs 0038-0044).

As to claim 2, the masking layer comprises a pad oxide layer (102)(page 2, paragraph 0033) and silicon nitride layer (103) thereon (figure 3) (page 3, paragraph 0037).

As to claim 11, Shimizu suggest a thermal oxidation for layer (115)(page 3, paragraph 0041).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US 2003/0143815) as applied to claims 1, 2 and 11 above, and further in view of Akatsu et al. (US 20050026382).

A difference is noted between applicant's claim 3 and the reference of Shimizu, the method of Shimizu, as described above, does not include a BSG layer as a hard mask on top of the said masking layer as claimed by the applicant (claim 3, page 10, line 3).

The reference of Akatsu discloses a method for improved trench processing where BSG (240) is used as a hard mask to pattern the said masking layer (page 3, paragraph 37, and figure 2). Process steps associated with the deposition and etch of the BSG layer are also described.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of reference Shimizu to include an additional BSG layer under the photoresist layer because the reference of Akatsu illustrates a hard mask is desirable because it prevents modification of the lithographic critical dimensions during the opening of the said masking layer as photoresist could be eroded or affected by the mask layer opening etch step. One of ordinary skill in the art would have been motivated to include an additional inorganic hard mask layer in order to obtain a better control of the critical dimensions as defined by the lithography in the photoresist mask. The BSG layer would improve mask etch selectivity.

As to claims 4, a difference is noted between applicant's claim 4 and the reference of Shimizu , Shimizu is silent about further removing a portion of the opening in the sidewall of the masking layer.

The reference of Akatsu discloses a method where etching is performed to pull back the pad stack (230) (page 4, paragraph 41) which reads-on "removing portions of the opening in the sidewalls",the removal of the BSG layer (240) is also described (page 5, paragraph 52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of reference Shimizu to include a mask pull back step because the reference of Akatsu teaches it is conventional to use mask pull back etch in order control the etch profile of the sidewalls. One of ordinary skill in the art would have been motivated to pull back the masking layer in order to obtain a tapered or rounded profile if desired. Applicant does not show unexpected results by using a conventionally used mask pull back step.

As to claim 13 and 14 the limitations regarding successively forming a pad oxide layer, a silicon nitride layer, successively etching the oxide layer to form at least one opening therein to expose the substrate and etching the exposed substrate to form a recess region in the substrate; oxidizing the recess region by thermal oxidation to form a first oxide layer thereon to round the top corner of the recess region; successively etching the first oxide layer and the substrate under the opening to form a trench in the substrate, conformably forming a second oxide layer on the surface of the trench, have been addressed above in relation to claim 1. The reference of Shimizu further discloses

filling the trench (107) with an insulating layer (109)(page 2, paragraph 0032) which is used to form a shallow trench structure.

A difference is noted between applicant's claim 13 and the reference of Shimizu, Shimizu, as previously discussed fails to disclose a boron silicate glass layer overlying a substrate and etching the boron silicate glass layer.

As discussed above, the reference of Akatsu discloses a method for improved trench processing where BSG (240) is used as a hard mask to pattern the said masking layer (page 3, paragraph 37, and figure 2). Process steps associated with the deposition and etch of the BSG layer are also described.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of reference Shimizu to include an additional BSG layer under the photoresist layer because the reference of Akatsu illustrates a hard mask is desirable because it prevents modification of the lithographic critical dimensions during the opening of the said masking layer as photoresist could be eroded or affected by the mask layer opening etch step. One of ordinary skill in the art would have been motivated to include an additional inorganic hard mask layer in order to obtain a better control of the critical dimensions as defined by the lithography in the photoresist mask. The BSG layer would improve mask etch selectivity. As to the sequence of the included process steps, one of ordinary skill in the art would have found it obvious to form the BSG layer after the nitride layer, and the etching of the BSG layer to be performed prior to etching the nitride layer because as suggested by Akatsu, the BSG layer is formed to pattern the nitride layer.

In regard to claim 14, As discussed above in reference to claim 4, Akatsu also discloses a method where etching is performed to pull back the pad stack (230) (page 4, paragraph 41) which reads-on "removing portions of the opening in the sidewalls", the removal of the BSG layer (240) is also described (page 5, paragraph 52). As to the sequence of the opening step, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of reference Shimizu to remove portions of the nitride mask sidewalls after the BSG layer has been removed and before forming layer (115) because the etch selectivity between the oxide and BSG is not large enough to allow BSG removal without oxide layer (115) simultaneous etch. One of ordinary skill in the art would have been motivated to perform the removal of the BSG layer separately from etching layer (115) in order to obtain a fine control of the second oxide etch step which is much more critical to the device operation than the removal of a mask layer.

6. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US 2003/0143815) in view of Akatsu et al. (US 20050026382) as applied to claims 3, 4, 13 and 14 above, and further in view of Fuller et al. (US 6174787).

The method of reference Shimizu modified by Akatsu, as described above is silent about the specific method for the mask layer pullback as described by applicant's claim 5.

Fuller discloses a silicon corner rounding method for shallow trench isolation where the masking layer (oxide and nitride) (104) is recessed or pulled-back using a HF/EG solution (column 4, lines 15-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of Shimizu and Akatsu to include the teachings of Fuller in order to obtain an isotropic etch for pulling back the mask layer. One of ordinary skill in the art would have been motivated to use HF or EG or a mixture in order to pull back the masking layer because, as indicated by Fuller, this method in conventionally used in semiconductor processing for rounding etch corners.

7. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US 2003/0143815) in view of Akatsu et al. (US 20050026382) as applied to claims 3, 4, 13 and 14 above, and further in view of Kim (KR 2003039385).

The modified method Shimizu, as described above is silent about the specific depth of the recess region as described by applicant's claims 6 and 16.

Kim describes a method for forming trench of semiconductor device to prevent damage of trench by forming rounded trench corner using a two step etch process where the substrate (10) is etched to the depth of 200-300 Angstroms by the first etch process (see abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further modify the process of Shimizu to include the teachings of Kim to remove 200 to 300 Angstroms from the substrate because removal

of the top substrate surface allows reduction of potential damage from top substrate surface (micro-scratches) and allows formation of rounded corner during first oxidation. The difference in ranges between applicant's claims 6 and 16 and the reference of Kim is within the etch depth control range. One of ordinary skill in the art would have been motivated to remove a thin layer (100-300 angstroms) of the substrate surface in order to improve damage performance of the resulting device.

Claims 7, 8, 9, 10, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US 2003/0143815) in view of Akatsu et al. (US 20050026382) as applied to claims 3, 4, 13 and 14 above, and further in view of Ajmera et al. (US 20020072196).

The method of reference Shimizu as described above discloses an oxidation layer (105) obtained by thermal oxidation.

A difference is noted between the applicant's claims and the reference of Shimizu which fails to specifically disclose a rapid thermal oxidation method for forming the said first oxide layer (105).

Ajmera discloses a shallow trench isolation method where the trench sidewalls ((16), figure 5) are oxidized using a rapid thermal oxidation (RTO) method performed at 1150°C for 30-200 seconds yielding an oxide thickness of 20-300 Angstroms (page 4, paragraph 32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of reference of Shimizu to

substitute an RTO step for a conventional oxidation furnace step, as rapid thermal processing (RTP) is becoming increasingly more available in semiconductor manufacturing facilities. One of ordinary skill in the art would have been motivated to use an RTO step to use equipment already available, thereby lowering the process time and cost of the manufactured chips. The RTP parameters would be adjusted within the parameter space suggested by Ajmera which include a temperature of 1150°C an oxidation time of 30-200 seconds yielding an oxide thickness of 20-300 Angstroms.

8. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (US 2003/0143815) as applied to claims 3, 4, 13 and 14 above, and further in view of Yoo et al. (US 6033969).

A difference is noted between the applicant's claim 12 and the reference of Shimizu, Shimizu discloses the (second) oxide layer (115) with a thickness of 300 angstroms.

Yoo discloses a method for forming a shallow trench isolation that has rounded and protected corners by first forming a bird's beak field oxide layer(50) prior to the trench-forming step such that a rounded and protected top corner (52) and a rounded bottom corner of the trench(62) can be formed. The top corner of the trench opening is protected by the beak portion of the bird's beak against etching in a subsequent oxide dip process before gate formation. As in the applicants claim 1, Yoo opens the pad oxide and nitride mask to expose the silicon substrate (column 2, line 53), the forming an oxide layer, the etching the oxide (column 2, line 59), and then

etching the silicon substrate (column 2, line 61). The oxide thickness disclosed by Yoo is about 100-200 Angstroms (Column 4, line 21) which includes the range claimed by the applicant.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the process of reference of Shimizu to include a thinner oxide layer (115) of about 100 angstroms (or more) because the reference of Yoo teaches oxidation film as thin as 100 angstroms, or more such as 110 to 140 angstroms, can be used for rounding corners. One of ordinary skill in the art would have been motivated to use about 110 to 140 angstroms oxidation for layer (115) in order to shorten the oxidation process time and cost while rounding the bottom corner of the trench.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mahmoud Dahimene

MD

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER